

Notice of Allowability	Application No.	Applicant(s)	
	09/747,194	YOKOYAMA, RYOICHI	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 07/11/05.
2. ☒ The allowed claim(s) is/are 10,12-27 and 50-56, renumbered as 1-24.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____. |

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Cancel non-elected claims 2-3, 5-8, 11, 40-49.

Cancel claims 28-39.

Authorization for this examiner's amendment was given in a telephone interview with Attorney John P. Scherlacher on 09.29.05.

Allowable Subject Matter

2. Claims 10, 12-27, 50-56 are allowed.

3. The following is an examiner's statement of reasons for allowance:

The present invention relates to a display apparatus, comprising:

a plurality of gate lines provided in one direction of a substrate;

a plurality of drain lines provided in a direction intersecting with said

gate lines; and

a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of said plurality of gate lines, and which is supplied with an image signal from corresponding one of said plurality of drain lines; wherein

each of said plurality of display pixels comprises:

a display element;

a first display circuit having a storing circuit, for storing a digital image signal from said corresponding one of drain lines in response to a scan signal from said corresponding one of gate lines, and a signal selector which is operated based on data stored at said storing circuit for selecting an output signal from among two or more display signals and supplying said selected signal to said display element; and

a second display circuit having a storage capacitor for storing an analog image signal from said corresponding one of drain lines in response to a scan signal from said corresponding one of gate lines, wherein the signal stored in said storage capacitor is supplied to said display element;

wherein said display pixel further comprises a display circuit selector for selectively supplying an image signal from said corresponding one of drain lines to said first or second display circuit;

and further including an output selector which selectively supplies data stored in one of said first display circuit and said second display circuit to said display element, as disclosed in claim 10. The closest art, Okumura et al., Akiyama et al., Toyo et al. disclose related displays, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

Claims 13-19, 21 and 50-53 depend on claim 10.

The invention is also concerns a display apparatus, comprising:

a plurality of gate lines provided in one direction of a substrate;

a plurality of drain lines provided in a direction intersecting with said

gate lines; and

a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of said plurality of gate lines, and which is supplied with an image signal from corresponding one of said plurality of drain lines; wherein

each of said plurality of display pixels comprises:

a display element;

a first display circuit having a storing circuit, for storing a digital image signal from said corresponding one of drain lines in response to a scan signal from said corresponding one of gate lines, and a signal selector which is operated based on data stored at said storing circuit for selecting an output signal from among two or more display signals and supplying said selected signal to said display element; and

a second display circuit having a storage capacitor for storing an analog image signal from said corresponding one of drain lines in response to a scan signal from said corresponding one of gate lines, wherein the signal stored in said storage capacitor is supplied to said display element;

wherein said display pixel further comprises a display circuit selector for selectively supplying an image signal from said first or second display circuit to display element, as disclosed in claim 12. The closest art, Okumura et al., Akiyama et al., Toyo et al. disclose related displays, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

The invention is also concerns a display apparatus, comprising:

a plurality of gate lines provided in one direction of a substrate;

a plurality of drain lines provided in a direction intersecting with said gate lines; and

a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of said plurality of gate lines, and which is supplied with an image signal from corresponding one of said plurality of drain lines; wherein

each of said plurality of display pixels comprises:

a display element;

a first display circuit having a storing circuit, for storing a digital image signal from said corresponding one of drain lines in response to a scan signal from said corresponding one of gate lines, and

a second display circuit having a storage capacitor for storing an analog image signal from said corresponding one of drain lines in response to a scan signal from said corresponding one of gate lines;

and further including an output selector which selectively supplies data stored in one of said first display circuit and said second display circuit to said display element, as disclosed in claim 20. The closest art, Okumura et al., Akiyama et al., Toyo et al. disclose related displays, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

Claim 54 depends on claim 10.

The invention is also concerns a display apparatus comprising a plurality of display pixels, wherein each of said plurality of display pixels comprises:

a pixel electrode;

a first storing circuit, for storing a digital data and outputting signals to said pixel electrode,

a second storing circuit for storing an analog data and outputting signals to said pixel electrode; and

and storing circuit selector for switching between said first and second circuits;
and further including an output selector which selectively supplies data stored
in one of said first display circuit and said second display circuit to said display element, as disclosed in claim 22. The closest art, Okumura et al., Akiyama et al., Toyo et al. disclose related displays, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

Claims 23-27 and 55-56 depend on claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
09.29.05

A handwritten signature in black ink, appearing to read 'Vijay Shankar', with a long, sweeping horizontal line extending to the right.

**VIJAY SHANKAR
PRIMARY EXAMINER**